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His current responsibilities include developing and managing assertions technology and other techniques for design verification. He holds three patents and has published many papers at conferences. He was a member of the IEEE P1800 System Verilog Assertions committee and a co-author of The Power

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What are Financial Statement Assertions?

He was a member of the IEEE P1800 System Verilog Assertions committee and a co-author of The Power of System Verilog Assertions (Springer 2010). John Havlicek earned a B.S. in Mathematics from Ohio State (1987) and a Ph.D. in

Mathematics from Stanford (1992).